Processor + SRAM

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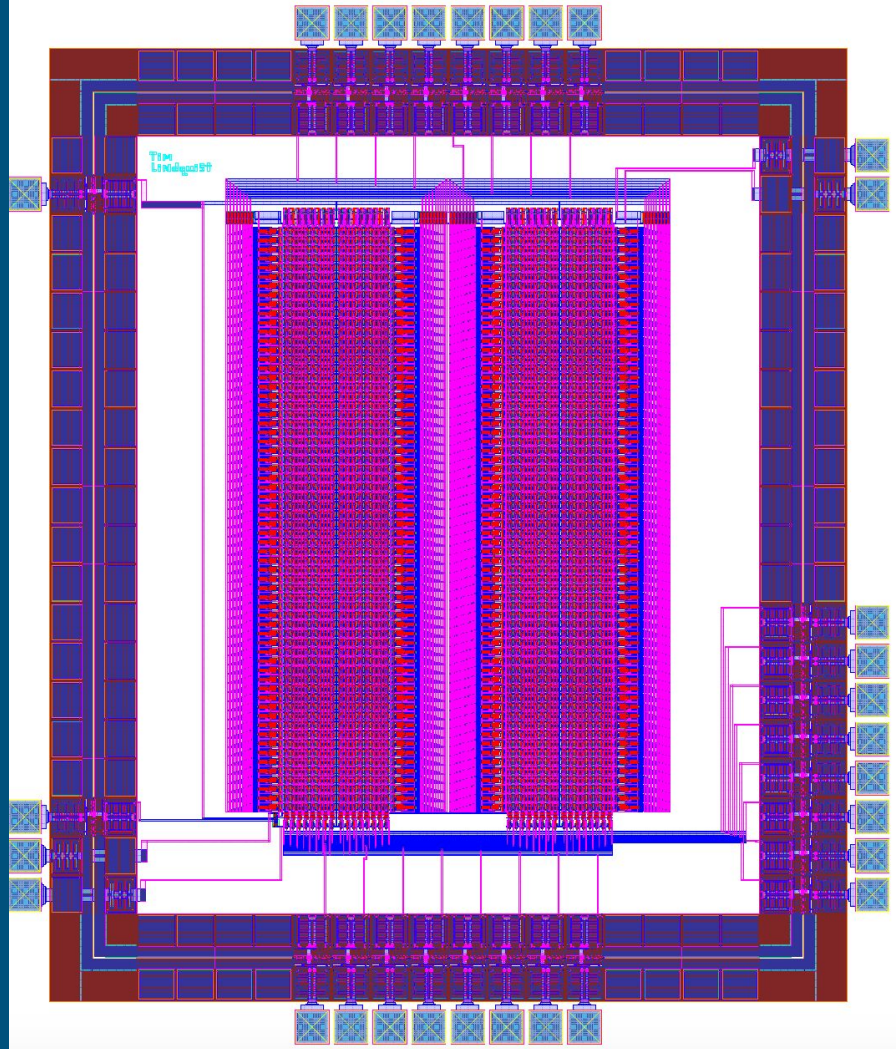
The SRAM



SRAM

REQUIREMENTS:

- 256x8bit
- 6T process
- Read/Write capability
- Data line precharging
- 1MHz CLK

The 6T Cell

6T=6 transistors

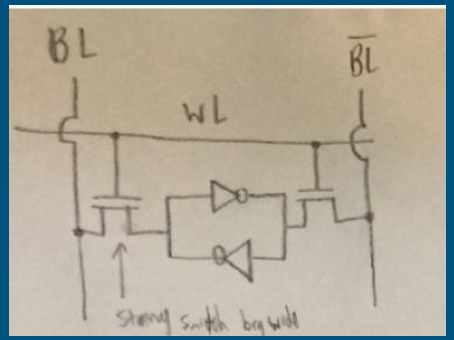
Store 1 bit (0 or 1)

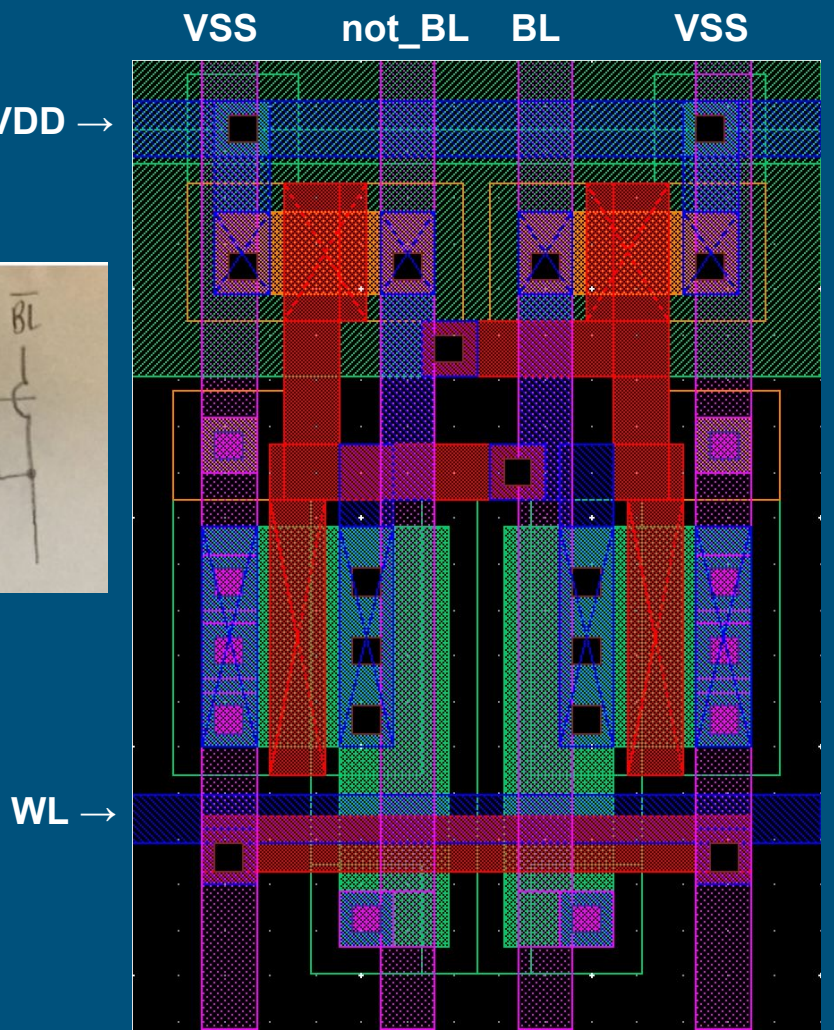
- Require 2048 cells

Sizing ratios

- PD transistors 8/2 λ
- Access transistors 4/2 λ
- PU transistors 3/3 λ

PD:4x Access: 2x PU:1x





The Write Drivers

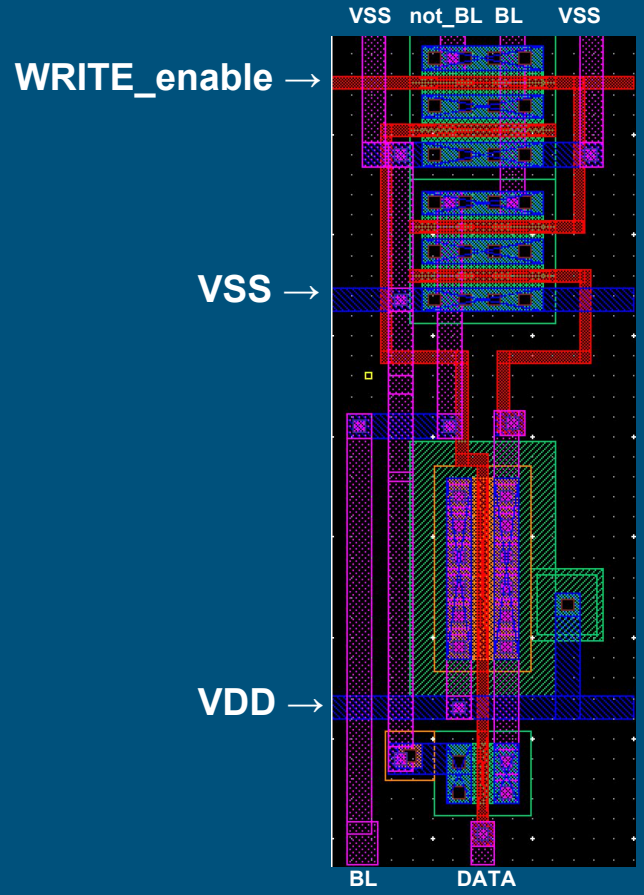
Placement:

- Under 6T cell
- 1 row x 8 column

Function

- Write data to BL’s
- Read data from BL’s

Strong Transistors



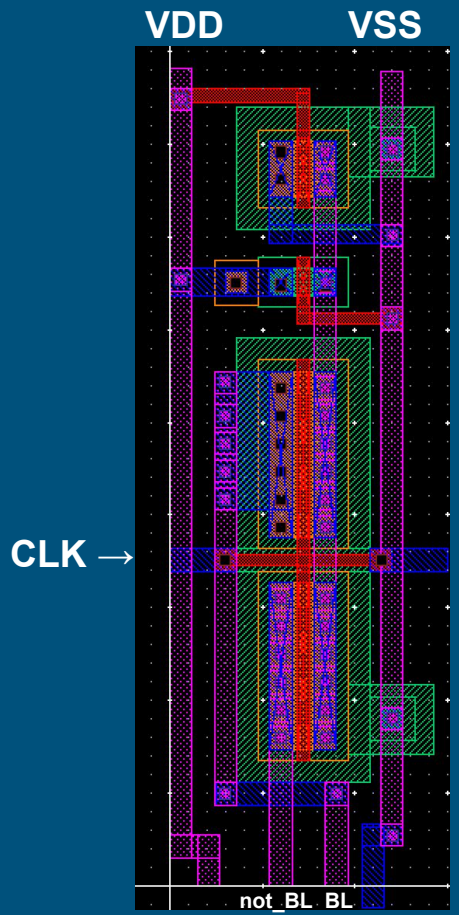
Precharge

Placement

- Above 6T cell
- 1row x 8 column

Function

- Charge line to VDD when CLK is low
- Conditions lines

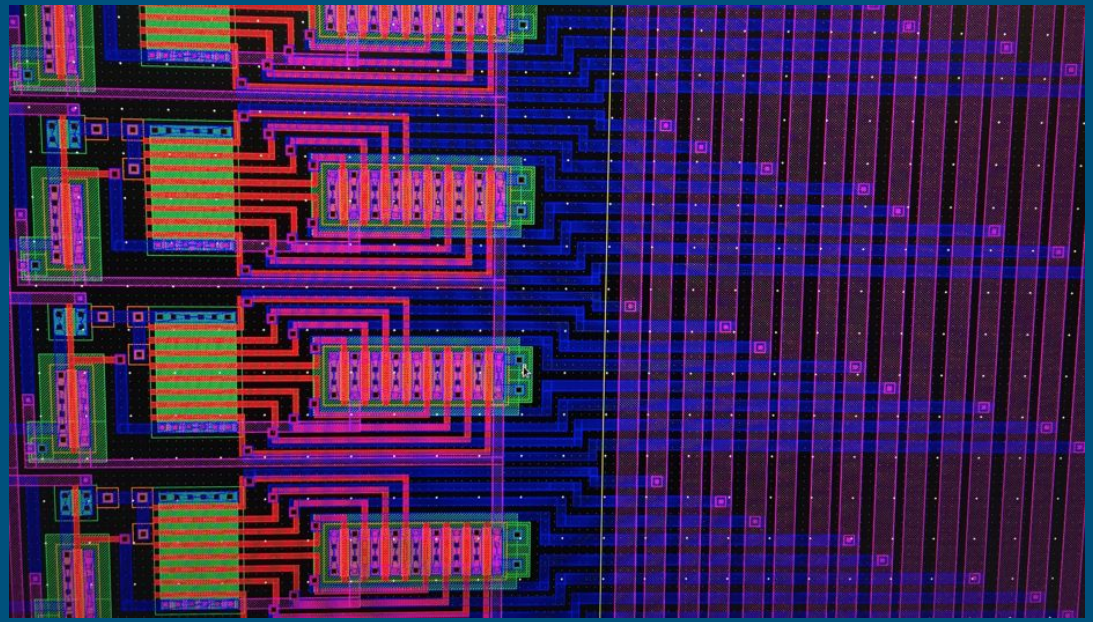


8 x 256 Decoder

8 input AND gate

Addressable 16 line config

256 different addresses



WRITE Operation

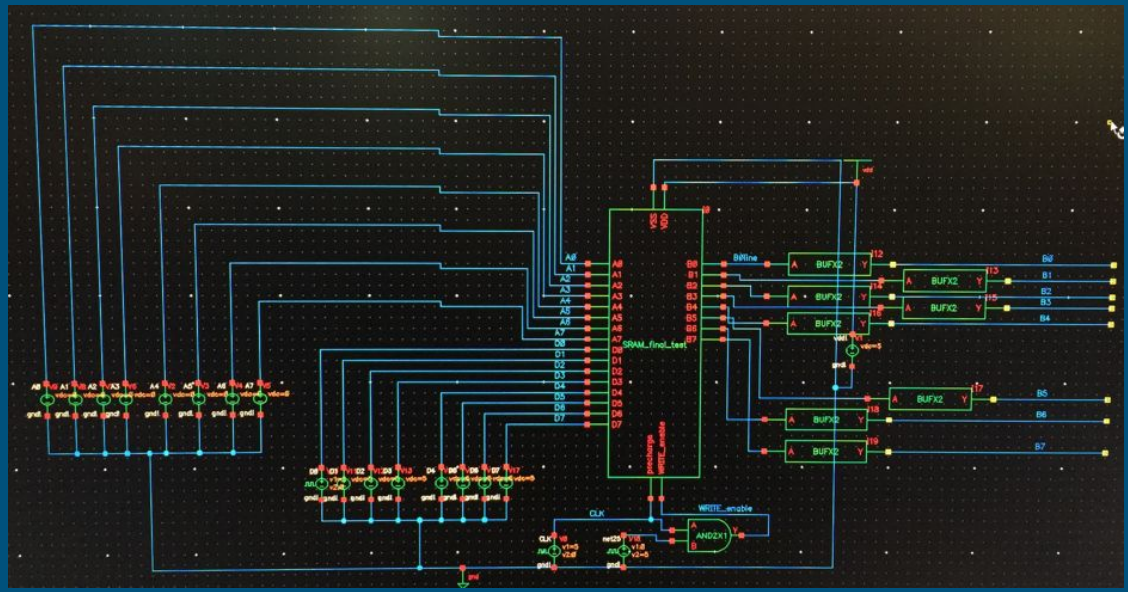
1. Write Drivers force BL and not_BL to desired state.
2. WL set to HIGH to turn on access transistors
3. Cell is written
4. WL drops LOW to save state

READ Operation

1. Precharge lines on lower CLK
2. CLK goes HIGH
3. WL set HIGH for desired address
4. Value read off BL
5. WL set to LOW

Testing

Environment= extracted parts

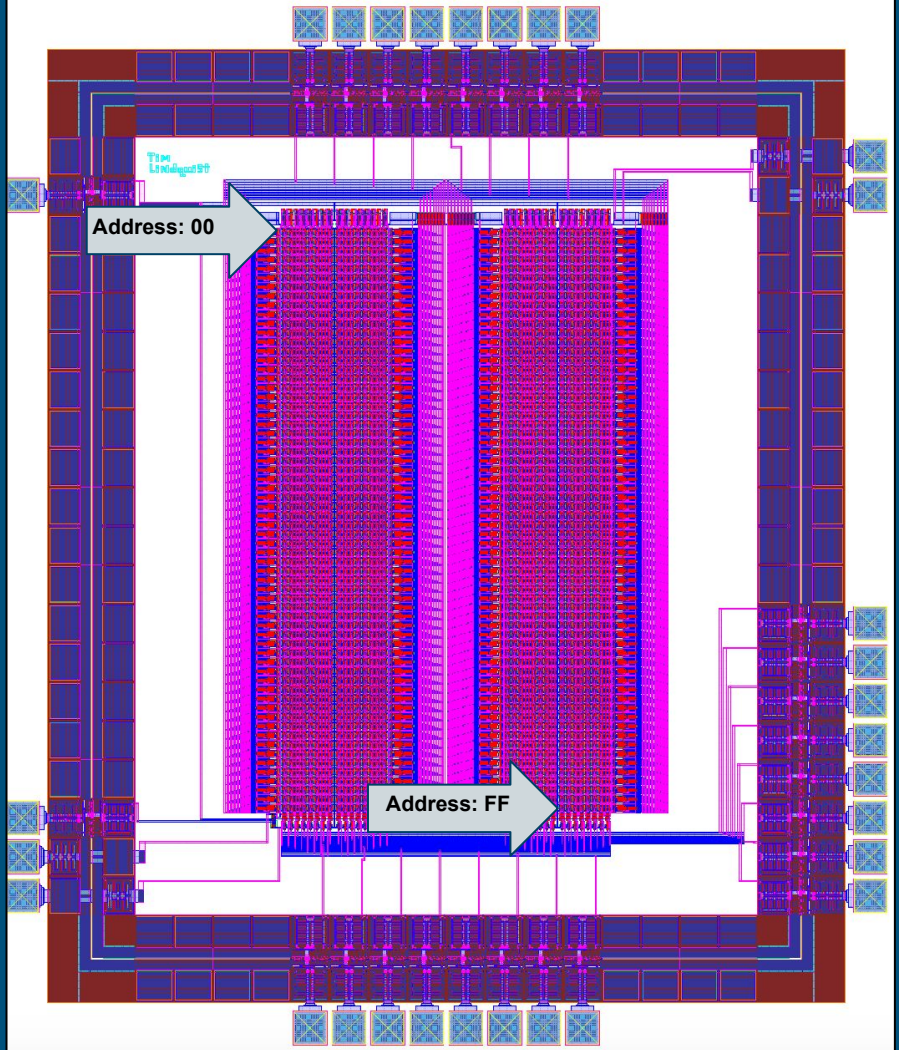


Results

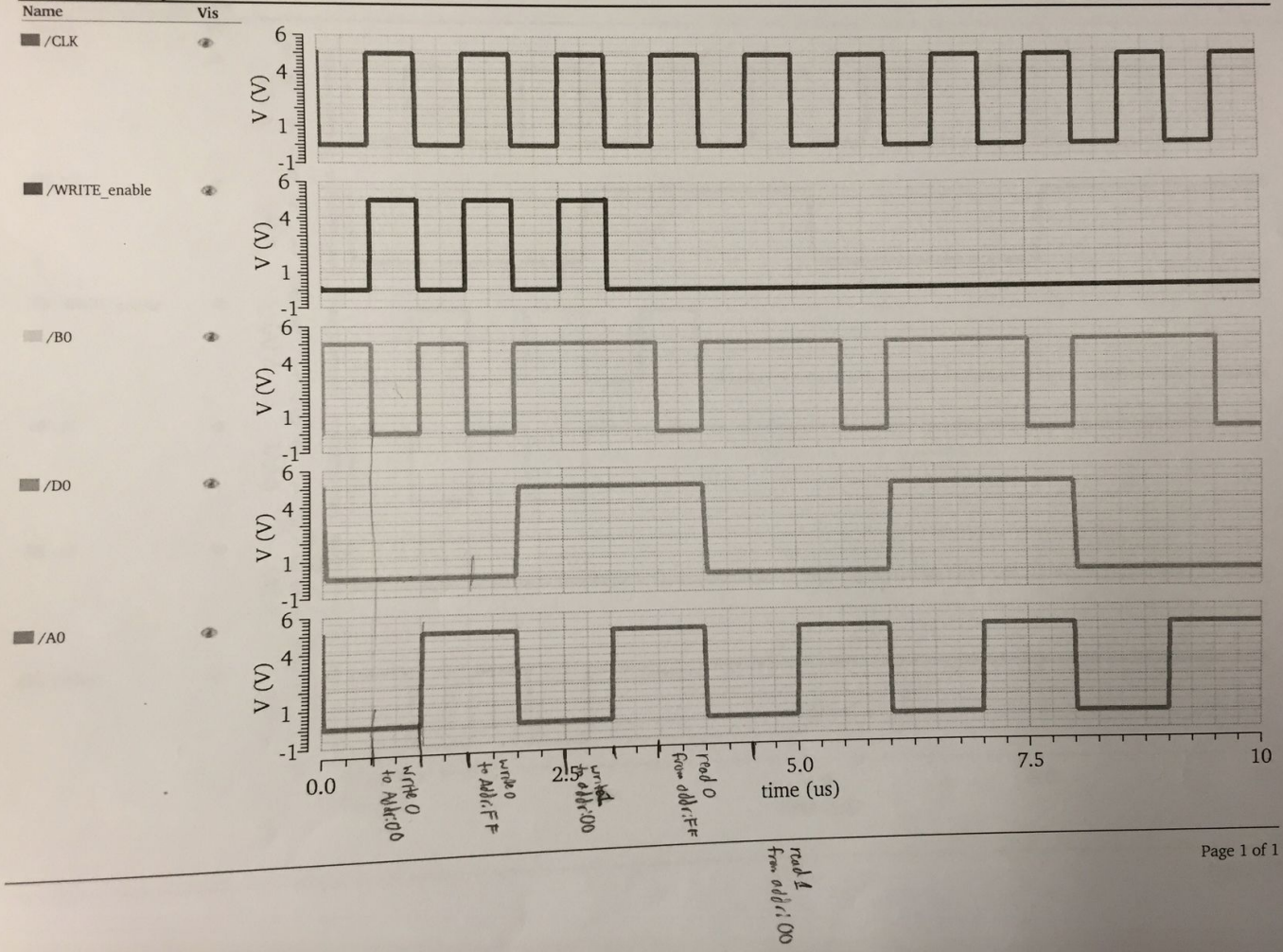
Successfully read & wrote into addr 00:FF

00=0000 0000

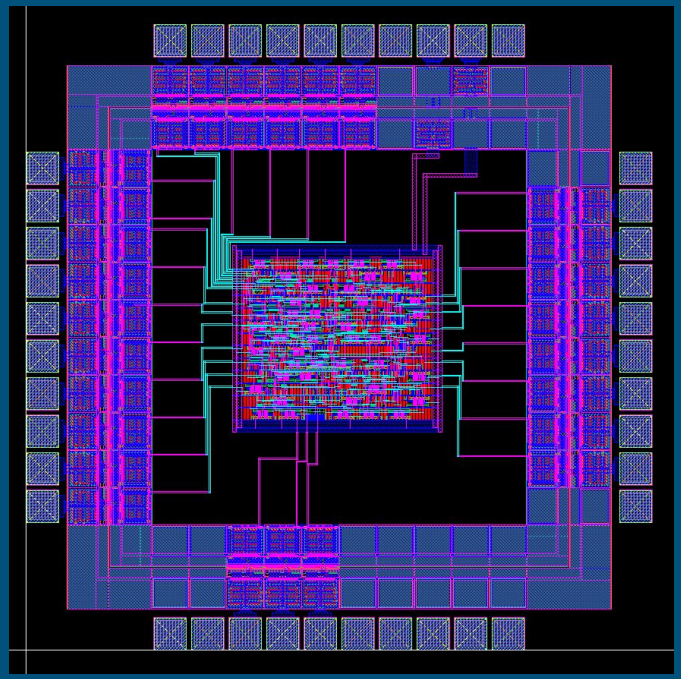
FF=1111 1111



Transient Response



SUBLEQ: Single-Instruction Processor



SUBLEQ

2486 Transistors

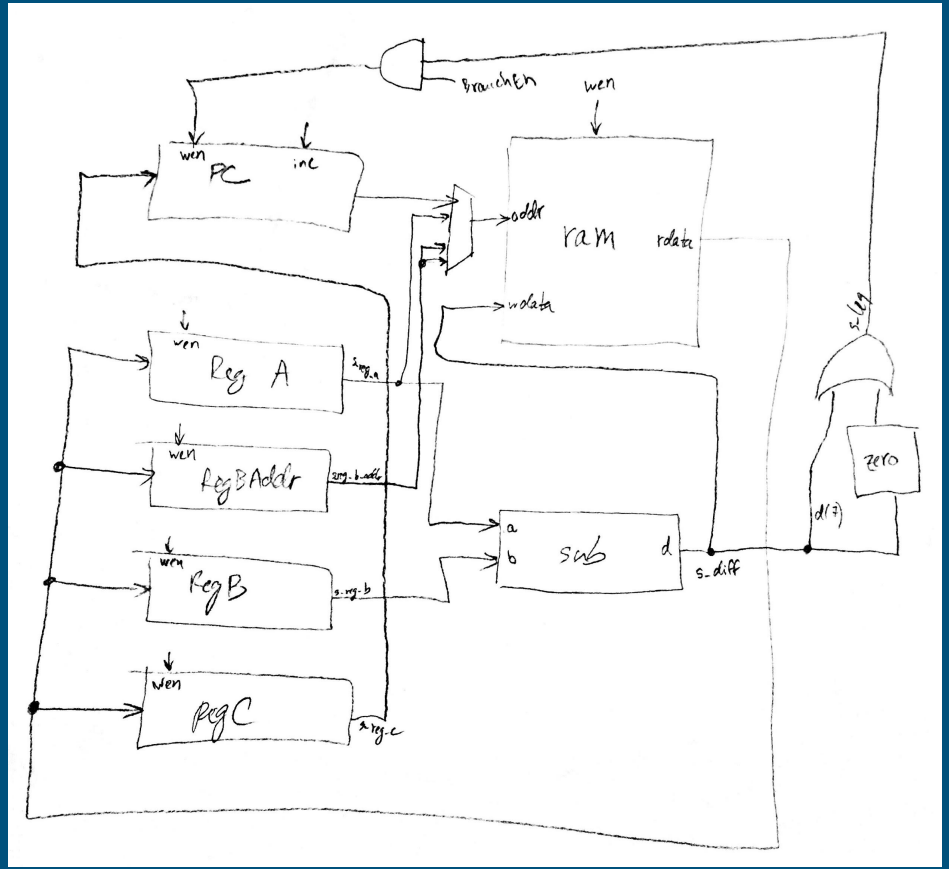
8-bit architecture

1 instruction

Low power

Extremely minimalistic computer architecture

Interesting concept



SUBLEQ

SUbtract A from B and Branch to C if result LEss or EQual to zero

Disable branch by making value C the same as NextPC

Force Jump by subtracting 0-0

Add by subtracting a negative number

Can solve any algorithmic problem*

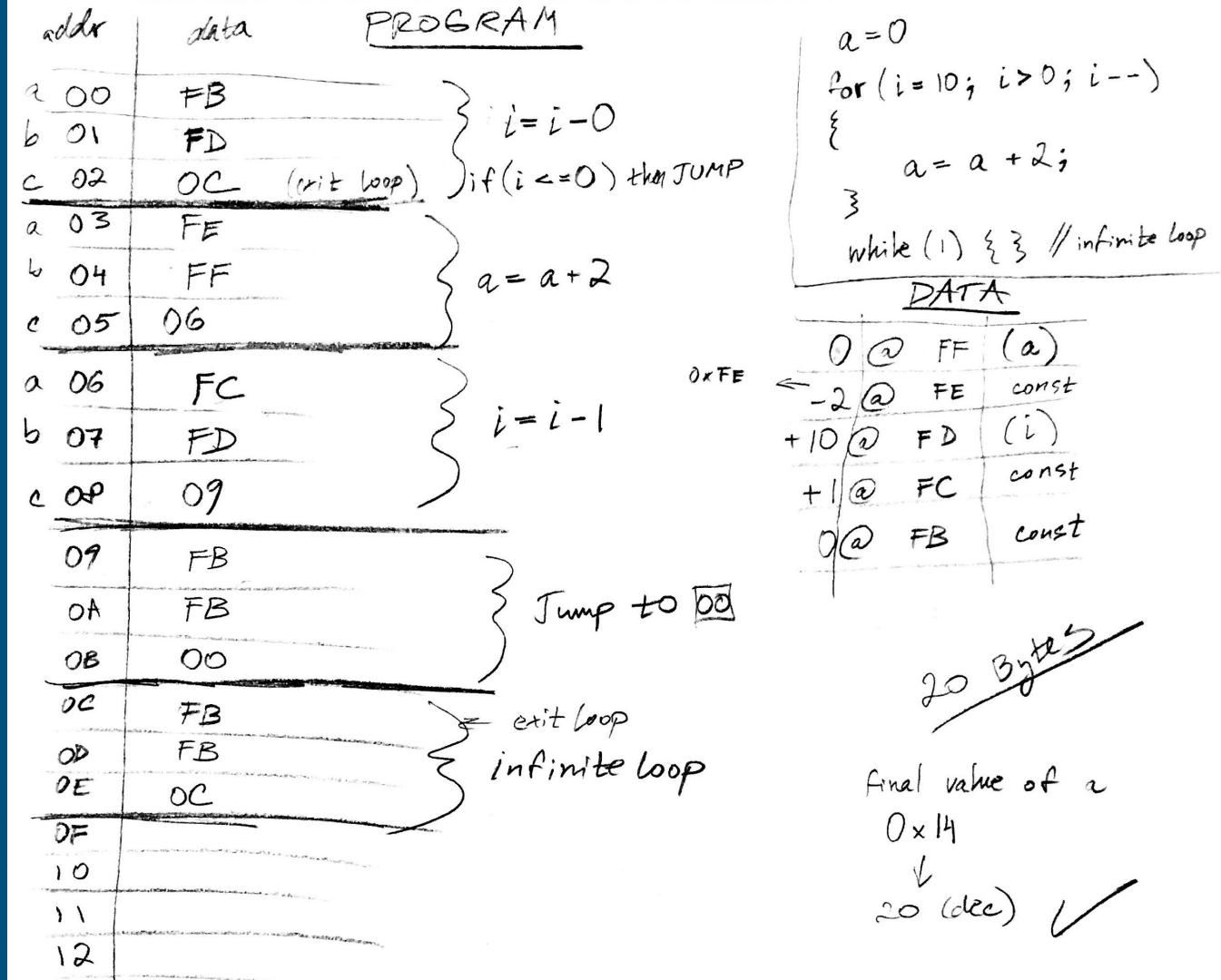
* (given enough memory...)

SUBLEQ: Where is the potential?

- Low component count has several effects
  - Lower propagation delays (higher clock speeds)
  - Low power
- Simplicity
  - Ideal where universal high performance not needed (ie. wrist watch)
  - Potential high performance in parallel setup

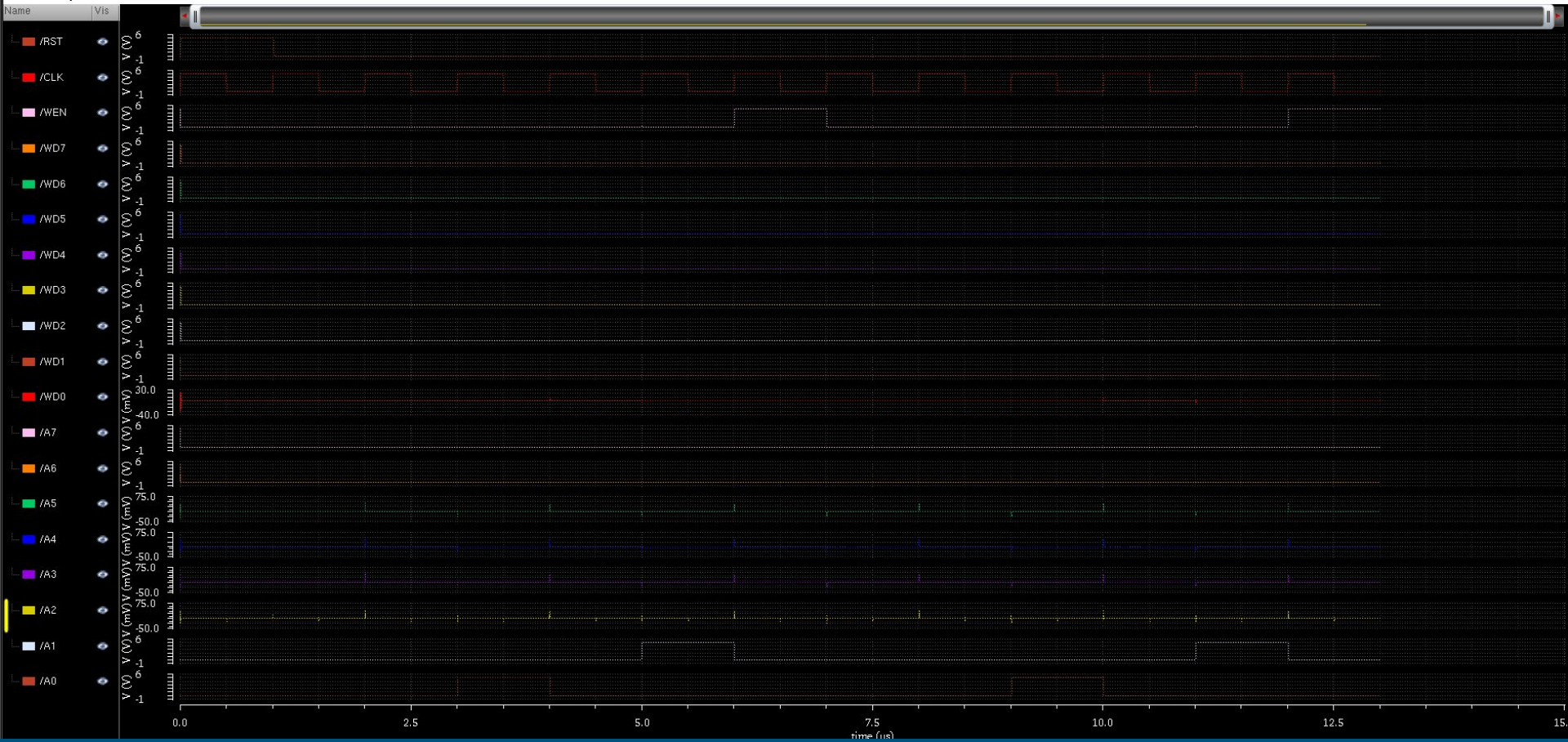
```
Total Power
--------------------------------------------------------------------------------
Total Internal Power:       1.836      67.16%
Total Switching Power:      0.8979      32.84%
Total Leakage Power:    3.78e-05   0.001382%
Total Power:       2.734
--------------------------------------------------------------------------------


Group                          Internal   Switching     Leakage       Total  Percentage
                               Power      Power         Power         Power  (%)
--------------------------------------------------------------------------------
Sequential                        1.382       0.124   2.292e-05       1.506       55.07
Macro                                 0           0           0           0           0
IO                                    0           0           0           0           0
Combinational                     0.339      0.4066   1.451e-05      0.7457       27.27
Clock (Combinational)            0.1154      0.3673   3.684e-07      0.4827       17.65
Clock (Sequential)                    0           0           0           0           0
--------------------------------------------------------------------------------
Total                             1.836      0.8979    3.78e-05       2.734         100
--------------------------------------------------------------------------------


Rail                 Voltage   Internal   Switching     Leakage       Total  Percentage
                               Power      Power         Power         Power  (%)
--------------------------------------------------------------------------------
Default                    5      1.836      0.8979    3.78e-05       2.734         100


Clock                          Internal   Switching     Leakage       Total  Percentage
                               Power      Power         Power         Power  (%)
--------------------------------------------------------------------------------
i_clk                             0.1154      0.3673   3.684e-07      0.4827       17.65
--------------------------------------------------------------------------------
Total                             0.1154      0.3673   3.684e-07      0.4827       17.65
--------------------------------------------------------------------------------


--------------------------------------------------------------------------------
*       Power Distribution Summary:
*              Highest Average Power:             i_clk__L2_I0 (INVX8):          0.1928
*              Highest Leakage Power: control_logic_current_state_reg[0] (DFFSR):       5.33e-07
*              Total Cap:      2.0638e-11 F
*              Total instances in design:   222
*              Total instances in design with no power:     0
*               Total instances in design with no activty:     0

*              Total Fillers and Decap:     0
--------------------------------------------------------------------------------
```

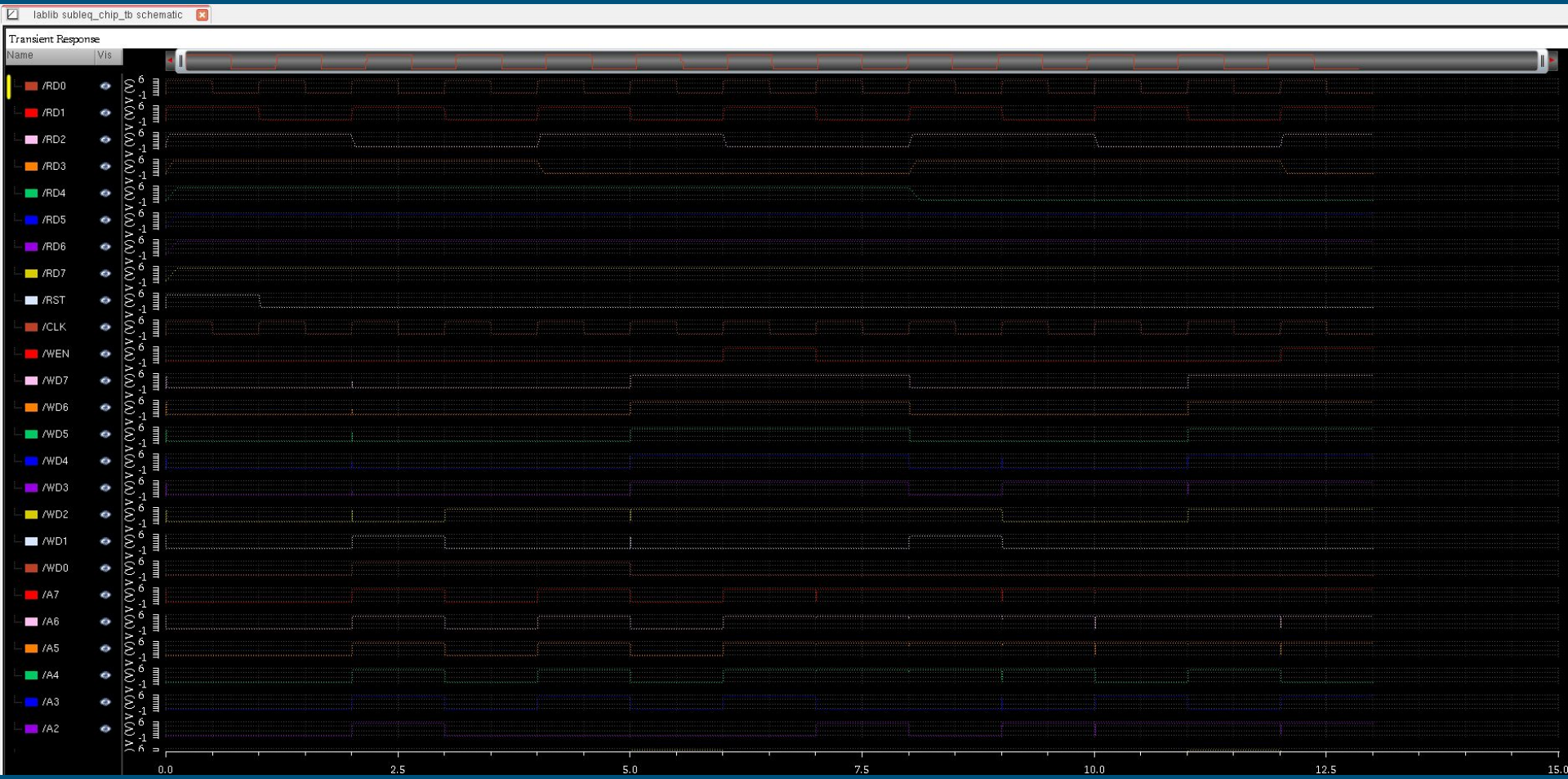
SUBLEQ: FPGA DEMO



lablib subleq_chip_tb schematic

Transient Response




lablib subleq_chip_tb schematic
Transient Response
Name
Vis
/RD0
/RD1
/RD2
/RD3
/RD4
/RD5
/RD6
/RD7
/RST
/CLK
/WEN
/WD7
/WD6
/WD5
/WD4
/WD3
/WD2
/WD1
/WD0
/A7
/A6
/A5
/A4
/A3
/A2
0.0
2.5
5.0
7.5
10.0
12.5
15.0